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SVPWM of High Power T-Type Three-Level Neutral-Point-Clamped Inverter

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Abstract
At present, the inverter is mainly two level topology. The three-level (3L) topology has the advantages of high voltage withstand level and low output current harmonics. However, because of the complexity of the modulation algorithm, the 3L topology is seldom used in high power inverters. In this paper, the space-vector-pulse-width-modulation (SVPWM) for 3L topology is studied. A 3L SVPWM is proposed, which is practical and easy to implement, and a 125kW 3L neutral-point-clamped (NPC) inverter is set up. The experimental results show that the proposed algorithm can effectively reduce harmonic current, which has some reference value for the application of high power 3L inverters.

Key words: Three-level, Neutral-point-clamped, Inverter, Space-vector-pulse-width-modulation, Current harmonics.

1. Introduction

The three-level neutral-point-clamped-inverter (3L-NPC) was proposed in 1981 [1], it has significant advantages over the conventional two-level voltage-source-inverter (2L-VSI): lower harmonic content and higher electrical energy quality at the same switching frequency; voltage stress across the switching devices is only half of the DC-bus voltage [2, 3]. Thus, the NPC has been widely used in small power and high voltage inverters. The pulse-width-modulation (PWM) methods for inverter are mainly classified into carrier-based-PWM (CBPWM) [4, 5] and space-vector-PWM (SVPWM) [6-10].

The conventional SVPWM for the 3L-NPC is developed on the basis of SVPWM of the 2L-VSI, so the existing SVPWM technology of the 2L-VSI can be used for the 3L-NPC. The drawback of SVPWM for the 3L-NPC is that it may cause a low frequency (thrice the fundamental frequency of the output voltage) oscillation of the neutral-point (NP) voltage under the conditions of high modulation indexes and low power factors [6], which can increase the voltage stress across switching devices and output voltage harmonics. Moreover, the 3L modulation algorithm is complicated and difficult to implement in engineering [7].

This thesis first studies the 3L-NPC modulation algorithm, and then a SVPWM method which is suitable for high power 3L inverter is proposed. Finally, the simulation and experiment are carried out.

1.1. Topology of T-type NPC

3L-NPC topology adds a neutral point freewheeling path and can output three levels of udc/2, 0 and -udc/2 by controlling the opening and closing of different switches. NPC inverter is divided into two types of T-type and I-type, the two topologies have exactly the same voltage vector space, that is, the same modulation algorithm can be applied at the same time on both. The difference is that the I-type 3L topology clamps with two

diodes, whereas the T-topology does not. The specific circuit modes of the two are slightly different. This paper takes T-type NPC as the analysis object.

T-type NPC inverter is shown in Fig.1. Each phase leg consists of four switches and four anti-parallel diodes. In Fig.1, udc is the DC supply voltage; C1 and C2 are the DC link capacitors; L is the filter inductance; R is equivalent resistance of filter inductance; O is the DC neutral point, and N is the AC neutral point.

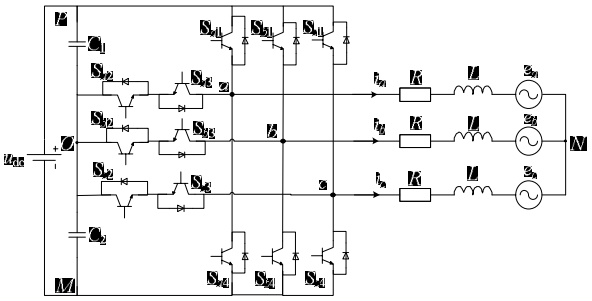


Figure 1. T-type NPC inverter

The switch function of the NPC inverter is defined to describe its voltage vector space:

$$S_{xn}=\begin{cases}\left(S_{x1},S_{x2},S_{x3},S_{x4}\right)=\left(1,1,0,0\right)=2\\ \left(S_{x1},S_{x2},S_{x3},S_{x4}\right)=\left(0,1,1,0\right)=1\\ \left(S_{x1},S_{x2},S_{x3},S_{x4}\right)=\left(0,0,1,1\right)=0\end{cases} \tag{1}$$

Where, Sxn = 1 means power switch tube x-th (x = a,b,c) of phase n-th (n = 1,2,3,4). Sxn = 1 indicates that the corresponding switch is turned on, and Sxn = 0 indicates that the corresponding switch is turned off.

The relationship between single phase output voltage and switching function is as follows:

$$\begin{cases}u_{aO}=\left(S_a-1\right)\dfrac{u_{\mathrm{dc}}}{2}\\ u_{bO}=\left(S_b-1\right)\dfrac{u_{\mathrm{dc}}}{2}\\ u_{cO}=\left(S_c-1\right)\dfrac{u_{\mathrm{dc}}}{2}\end{cases} \tag{2}$$

Where, is used to represent the switching state of three phase bridge arm. By the Kirchhoff's voltage law, the voltage equations of the three phase bridge arm are as follows:

$$\begin{cases}L\dfrac{di_a}{dt}+Ri_a=e_a-(u_{aO}+u_{OM}+u_{MN})\\ L\dfrac{di_b}{dt}+Ri_b=e_b-(u_{bO}+u_{OM}+u_{MN})\\ L\dfrac{di_c}{dt}+Ri_c=e_c-(u_{cO}+u_{OM}+u_{MN})\end{cases} \tag{3}$$

For a three phase balanced system, ea + eb + ec = 0, ia + ib +ic = 0, so the following equation is obtained:

$$u_{ON}=-\frac{1}{6}u_{\mathrm{dc}}\sum_{x=a,b,c}\left(S_x-1\right) \tag{4}$$

1.2. Vector Space Division

According to $3^3 = 27$ different combinations of switch states, make them correspond to a complex plane, the space vector distribution of the 3L inverter can be obtained as shown in Fig.2. The 27 switch states correspond to 27 space vectors, and the relation between the amplitude and phase of each vector can be seen clearly in Fig.2.

There are two ways to divide the sector of 3L space vector. The similarities between the two ways are that they divide the

space vector into 6 large sectors in the same way. The difference is that one method divides a large sector into 6 small sectors, and the other divides a large sector into 4 small sectors. The larger the number of small sectors, the more switching states used to synthesize reference vectors, which lead to the smaller output voltage harmonics, but the more complex the calculation process is. In this paper, a large sector has been divided into 6 small sectors as shown in Fig.2.

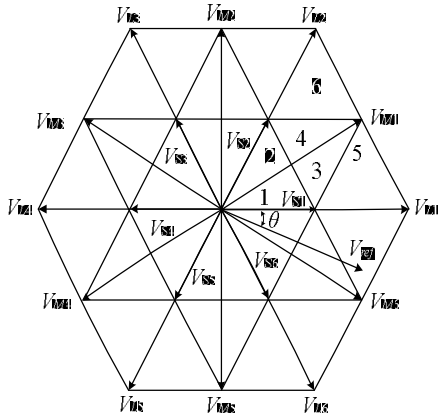


Figure 2. Vector space of 3L inverter

According to the length of those vectors in Fig.2, they can be divided into the 6 large vector VLx, 6 medium vector VMx, 12 small vector VSx and 3 zero vector V0 [8]. VLx, VMx, VSx and V0 (x = 1,2,3,4,5,6) respectively express each large, medium, small and zero vector. Each corresponds to two small redundant vectors, they produce the same reference voltage, such as (100) and (211) is a pair of small redundant vectors.

The expression of AC side output voltage produced by 27 switching states can be obtained by Eq.(4), as shown in Tab.1, in which the Vref is the space vector synthetized by the output phase voltage of the three phase bridge arm.

Table 1. Vector table of 3L NPC

Sa	Sb	Sc	uaN	ubN	ucN	Vref	Vector
0	0	0	0	0	0	000	Zero
0	0	1	$-\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	$\frac{1}{3}u_{dc}$	001	Small
0	0	2	$-\frac{1}{3}u_{dc}$	$-\frac{1}{3}u_{dc}$	$\frac{2}{3}u_{dc}$	002	Large
0	1	0	$-\frac{1}{6}u_{dc}$	$\frac{1}{3}u_{dc}$	$-\frac{1}{6}u_{dc}$	010	Small
0	1	1	$-\frac{1}{3}u_{dc}$	$\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	011	Small
0	1	2	$-\frac{1}{2}u_{dc}$	0	$\frac{1}{2}u_{dc}$	012	Medium
0	2	0	$-\frac{1}{3}u_{dc}$	$\frac{2}{3}u_{dc}$	$-\frac{1}{3}u_{dc}$	020	Large
0	2	1	$-\frac{1}{2}u_{dc}$	$\frac{1}{2}u_{dc}$	0	021	Medium
0	2	2	$-\frac{2}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	022	Large
1	0	0	$\frac{1}{3}u_{dc}$	$-\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	100	Small
1	0	1	$\frac{1}{6}u_{dc}$	$-\frac{2}{3}u_{dc}$	$\frac{1}{6}u_{dc}$	101	Small
1	0	2	0	$-\frac{1}{2}u_{dc}$	$\frac{1}{2}u_{dc}$	102	Medium
1	1	0	$\frac{1}{6}u_{dc}$	$\frac{1}{6}u_{dc}$	$-\frac{1}{3}u_{dc}$	110	Small
1	1	1	0	0	0	111	Zero
1	1	2	$-\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	$\frac{1}{3}u_{dc}$	112	Small

1	2	0	0	$\frac{1}{2}u_{dc}$	$-\frac{1}{2}u_{dc}$	120	Medium
1	2	1	$-\frac{1}{6}u_{dc}$	$\frac{1}{3}u_{dc}$	$-\frac{1}{6}u_{dc}$	121	Small
1	2	2	$-\frac{1}{3}u_{dc}$	$\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	122	Small
2	0	0	$\frac{2}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	200	Large
2	0	1	$\frac{1}{2}u_{dc}$	$-\frac{1}{2}u_{dc}$	0	201	Medium
2	0	2	$\frac{1}{3}u_{dc}$	$-\frac{2}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	202	Large
2	1	0	$\frac{1}{2}u_{dc}$	0	$-\frac{1}{2}u_{dc}$	210	Medium
2	1	1	$\frac{1}{3}u_{dc}$	$-\frac{1}{6}u_{dc}$	$-\frac{1}{6}u_{dc}$	211	Small
2	1	2	$\frac{1}{6}u_{dc}$	$-\frac{1}{3}u_{dc}$	$\frac{1}{6}u_{dc}$	212	Small
2	2	0	$\frac{1}{3}u_{dc}$	$\frac{1}{3}u_{dc}$	$-\frac{2}{3}u_{dc}$	220	Large
2	2	1	$\frac{1}{6}u_{dc}$	$\frac{1}{6}u_{dc}$	$\frac{1}{3}u_{dc}$	221	Small
2	2	2	0	0	0	222	Zero

As shown in Fig.2, the six large vectors divide the voltage space into six large sectors (I / II / III / IV / V / VI). Each big sector is divided into six small sectors (1/2/3/4/5/6) by the medium vector, the small vector, and the zero vector, which are located in a large sector. According to the sector of the reference voltage vector Vref, select the corresponding vector to composite Vref. The specific laws of choice are: (1) When the reference vector is located in the first and second small sectors, select two adjacent small vectors and zero vector to compose Vref; (2) When the reference vector is located in the third and fourth small sectors, two adjacent small vectors and an adjacent medium vector are needed to synthetize Vref; (3) When the reference vector is located in the 5th and 6th sector, choose a small vector, a medium vector and a large vector. The action time of each vector is determined by the principle of voltage second balance [8] and the seven-segment symmetrical SVPWM is adopt [9].

2. Implementation of SVPWM for T-NPC

In this paper, large sectors are represented by Rome numbers, and small sectors are represented by Arabia numbers. For example, III.4 represents fourth small sectors in the third lager sectors. In the modulation process, it is first necessary to determine the sector which the reference voltage vector $\boldsymbol{V}_{ref} = |\boldsymbol{V}_{ref}|e^{\vartheta}$ located.

2.1. Sector Judgment

With the advancement in networking and multimedia technologies enables the distribution and sharing of multimedia content widely. In the meantime, piracy becomes increasingly rampant as the customers can easily duplicate and redistribute the received multimedia content to a large audience. Insuring the copyrighted multimedia content is appropriately used has become increasingly critical.

First, determine the large sector in which the $\boldsymbol{V}_{ref}$ is located. It can be seen from Fig.2 that the large sector of the $\boldsymbol{V}_{ref}$ can be determined according to the phase angle theta θ of the $\boldsymbol{V}_{ref}$. For example, when $0 < \theta \leq \pi/3$, Vref locates in the large sector I, and the other large sectors are equally reasonable. After the large sector is judged, mapping all the large sectors to a large sector will simplify the calculation. In the case of mapping to the large sector I, the transformation formula is:

$$\theta' = \theta - \frac{\pi}{3} * (k-1) \tag{5}$$

In the Eq.(5), θ' is the phase angle of Vref after mapping to the large sector I; k is the large sector number of the Vref, k = (1,2,3,4,5,6).

Let the x = | Vref |cosθ and y = | Vref |sinθ are the components of Vref in the two phase stationary coordinate frame, respectively, and the small sector judgment rule is shown in Fig.3 [8].

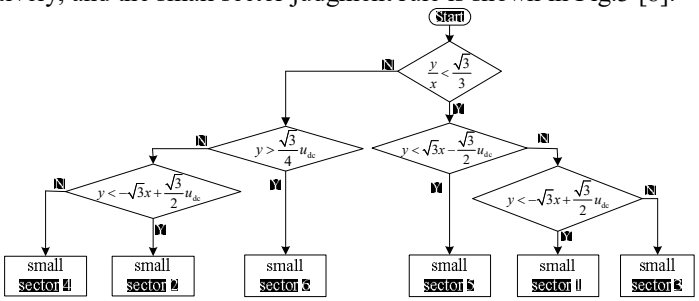


Figure 3. Judgment rule of a small sector

2.2. Vector Selection and Action Sequence

After the sector where Vref located is obtained, the Vref can be synthesized by the output voltage vector of the inverter, the commonly used method of synthesizing Vref is the nearest-three-vector (NTV) [6]. The advantage of NTV is that it can reduce the harmonic of the output voltage, common mode voltage and voltage stress of power devices. As shown in Fig.2, the Vref vertex is located in the sector VI.6, and the small sector is surrounded by the vertices of VS1, VM6 and VL1, so Vref can be synthesized by these three vectors.

After determining the three vectors used, the vector action sequence needs to be arranged. The principle mainly has three [10]: (1) to reduce the switching loss, each time the Vref changes, only one switch tube acts of each phase bridge; (2) to reduce the common mode voltage, the vector action sequence is symmetric; (3) the sequence of vectors should be helpful to reduce the fluctuation of neutral point potential of DC bus capacitor. In order to reduce the voltage stress of the switch device, the 3L modulation usually chooses the small vector as the starting vector, while the 2L modulation takes zero vector as the starting vector.

From the above discussion, the small vector nearest to Vref is arranged at the beginning and end of each modulation period, so that when the Vref changes, there is only one switch tube operates in each phase bridge arm, and the narrow pulse can be avoided as far as possible [2].

In this paper, the seven-segment symmetric vector action sequence is used, for example, the vector action sequence of VI.6 is 100-200-201-211-201-200-100.

2.3. Vector Action Time

The calculation method of 3L synthesis vector time is similar to the 2L SVPWM, they are all based on the volt second balance principle. Define V1, V2 and V3 are three vectors for Vref synthesis, T1, T2 and T3 are the action time of the three vectors respectively, and Ts is the modulation period. By the principle of volt second balance, the following equations are obtained [6]:

$$\begin{cases} V_1T_1 + V_2T_2 + V_3T_3 = V_{ref}T_s \\ T_1 + T_2 + T_3 = T_s \end{cases} \tag{6}$$

Taking sector I.1 as an example, and the sine theorem is applied to the small triangle composed of Vref, which as shown in the following equation:

$$\frac{V_{ref}}{\sin\frac{2}{3}\pi} = \frac{\frac{T_{100}}{T_s}V_{100}}{\sin(\frac{1}{3}\pi - \theta)} = \frac{\frac{T_{110}}{T_s}V_{110}}{\sin\theta} \tag{7}$$

The action time of each vector can be obtained from the Eq. (7). In order to reduce the computation, all the large sectors can be mapped to the first large sector I, so only vector action time of the large sector I is calculated. The following table is a vector table for each sector to synthesize vectors V1, V2 and V3.

Table 2. Synthetic vector table

Sector	V_1	V_2	V_3
I.1	V_{S1}	V_{S2}	V_0
I.2	V_{S2}	V_0	V_{S1}
I.3	V_{S1}	V_{S2}	V_{M1}

I.4	V_{S2}	V_{M1}	V_{S1}
I.5	V_{S1}	V_{L1}	V_{M1}
I.6	V_{S2}	V_{M1}	V_{L2}
II.1	V_{S2}	V_{S3}	V_0
II.2	V_{S3}	V_0	V_{S2}
II.3	V_{S2}	V_{S3}	V_{M2}
II.4	V_{S3}	V_{M2}	V_{S2}
II.5	V_{S2}	V_{L2}	V_{M2}
II.6	V_{S3}	V_{M2}	V_{L3}
III.1	V_{S2}	V_{S4}	V_0
III.2	V_{S4}	V_0	V_{S3}
III.3	V_{S3}	V_{S4}	V_{M3}
III.4	V_{S4}	V_{M3}	V_{S3}
III.5	V_{S3}	V_{L3}	V_{M3}
III.6	V_{S4}	V_{M3}	V_{L4}
IV.1	V_{S4}	V_{S5}	V_0
IV.2	V_{S4}	V_0	V_{S4}
IV.3	V_{S4}	V_{S5}	V_{M4}
IV.4	V_{S5}	V_{M4}	V_{S4}
IV.5	V_{S4}	V_{L4}	V_{M4}
IV.6	V_{S5}	V_{M4}	V_{L5}
V.1	V_{S5}	V_{S6}	V_0
V.2	V_{S6}	V_0	V_{S5}
V.3	V_{S5}	V_{S6}	V_{M5}
V.4	V_{S6}	V_{M5}	V_{S5}
V.5	V_{S5}	V_{L5}	V_{M5}
V.6	V_{S6}	V_{M5}	V_{L6}
VI.1	V_{S6}	V_{S6}	V_0
VI.2	V_{S1}	V_0	V_{S6}
VI.3	V_{S6}	V_{S1}	V_{M6}
VI.4	V_{S1}	V_{M6}	V_{S6}
VI.5	V_{S6}	V_{L6}	V_{M6}
VI.6	V_{S1}	V_{M6}	V_{L1}

For sector I.1, vector action times of V1, V2, and V3 are $T_{S1}= -2mT_s \sin(\vartheta'-\pi/3)$, $T_{S2}=2mT_s \sin\vartheta'$ and $T_0=T_s-T_{S1}-T_{S2}$ respectively, m is the modulation ratio, $m = \sqrt{3}|V_{ref}|/(3u_{dc})$.

3. Simulation and Experiment

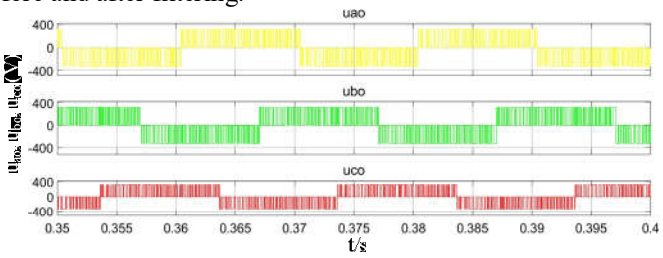
3.1 Simulation

The MATLAB/Simulink simulation model is built, and the simulation parameters are shown in Tab.3. The control strategy adopts the current loop control based on PI controller.

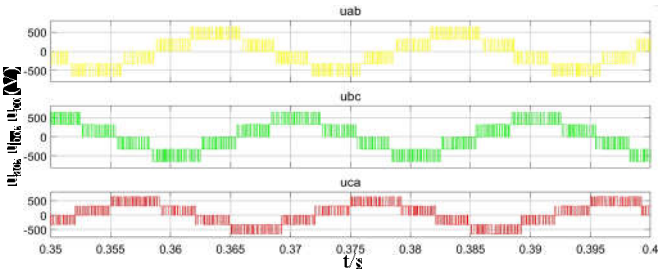
Table 3. Main parameters of simulation model

Item	Paramete r values	Parameter values	Parameter values
Rated power	125kVA	DC bus capacitor	2600uF
Switching frequency	5kHz	Filter inductor	0.4mH
DC Bus Voltage	600V	AC filter capacitor	100uF

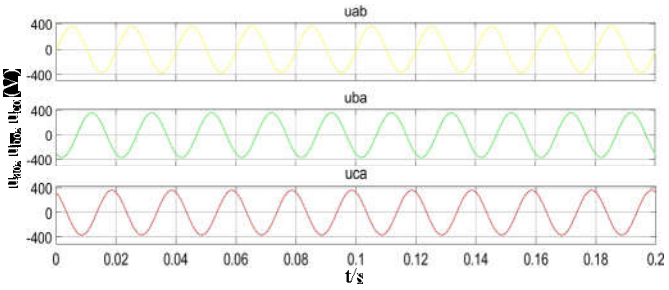
The simulation condition is the grid-connected mode, and the fundamental frequency is 50Hz. Fig.4 is output voltage waveforms before and after filtering.



(a) Output phase voltage before filtering



(b) Output line voltage before filtering



(c) Output line voltage after filtering

Figure 4. Simulation voltage waveforms

The simulation result shows that the output line voltage of the 3L topology has 5 electrical levels. Compared with the 2L topology, the advantage of 3L topology is that voltage and current harmonics are smaller and the power quality is better.

3.2 Experiment

A prototype of the T-NPC inverter is developed, the experimental condition is also under grid-connected mode. The control method is the same as the simulation and ignores the effects of neutral point potential fluctuation. The parameters are shown in the following table.

Table 4. Parameters of the experiment

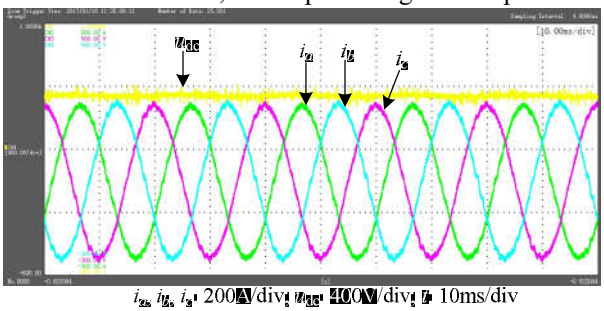
Item	Parameter values

Rated power	125kVA
IGBT	Semikron, KiM601TMLI12E4B
DC bus	550 V
Output AC voltage	270 V
DC bus capacitor	2600μF
Filter inductor	0.4 mH
Dead Time	3 us
DSP	TI, TMS320F28335
Oscilloscope	Yokogawa, DLM9040
Power quality analyzer	FLUKE, 1760

Fig.5 shows the internal structure of the power module. The module design adopts a modular design method which can effectively reduce the stray inductance of the line.

Figure 5. 125kW T-type power module

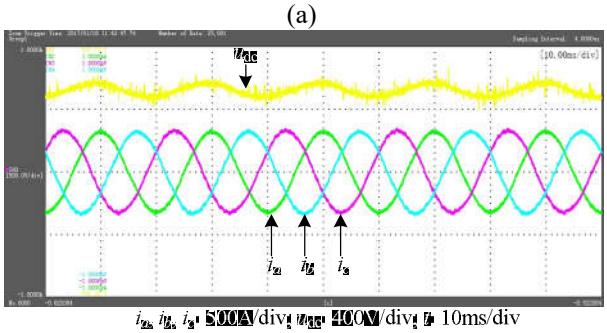
Fig.6 shows the experimental waveforms of the prototype. Channel 1 is DC bus voltage, channels 2, 3 and 4 are three phase output current of the prototype respectively. Due to the soft output characteristic of the DC power, when output power of the inverter is 125kW, the output voltage of DC power fluctuates.



i_{g1}, i_{g2}, i_{g3}: 200A/div; u_{dc}: 400V/div; T: 10ms/div

(a) Output power 83kW

(a)



i_{g1}, i_{g2}, i_{g3}: 500A/div; u_{dc}: 400V/div; T: 10ms/div

(b) Output power 125kW

Figure 6. Experimental waveform

Tab.5 show the harmonic content of output current in Fig.6(b), THD of ia, ib and ic is 2.5%, 2.12% and 2.37%, respectively. DC component of ia, ib and ic is 0.3259, 0.3027 and 0.0924, respectively. It can be seen that the output current harmonic of NPC inverter is very small.

Table 5. Harmonic content of output current

Item	phase a	phase b	phase c
THD/%	2.5	2.12	2.37
DC component	0.3259	0.3027	0.0924
2	0.03379	0.03345	0.03008
3	0.09907	0.24349	0.20044
4	0.03350	0.03375	0.03734
5	0.39539	0.45692	0.41107
6	0.02398	0.04805	0.03641
7	0.36320	0.35325	0.29337
8	0.03410	0.02116	0.03206
9	0.06889	0.03492	0.06465
10	0.02818	0.03407	0.03047
11	0.40232	0.42404	0.46015
12	0.04722	0.03167	0.05210
13	0.25470	0.29334	0.23107
14	0.05881	0.03166	0.05517
15	0.03664	0.04387	0.04796
16	0.05747	0.05549	0.05976
17	0.19315	0.10326	0.22811
18	0.02900	0.04007	0.03728
19	0.29610	0.24557	0.08699
20	0.11020	0.09642	0.13921
21	0.11771	0.23634	0.18890
22	0.14891	0.16100	0.13964
23	0.44445	0.33868	0.55420
24	0.05016	0.07026	0.06416
25	0.06945	0.06475	0.04478
26	0.05731	0.03756	0.04191
27	0.03298	0.02663	0.02991
28	0.04471	0.03735	0.04256
29	0.04773	0.02015	0.04880
30	0.02498	0.02241	0.01430

4. Conclusions

The modulation algorithm has a great influence on the power quality and performance of 3L NPC inverter. This paper briefly introduces the 3L grid-connected inverter, studies the performance of SVPWM algorithms, and introduces in detail the principle, implementation and performance analysis of the typical SVPWM algorithms for 3L NPC inverter. The simulation and experiment are carried, and some useful results are obtained.

1) A SVPWM algorithm is designed, which is suitable for high power T-type inverter and easy to implement in engineering.

2) A T-type NPC prototype is built by modular design method, and the experimental results show that the NPC inverter topology can effectively improve power quality and reduce the harmonic pollution.

3) The current harmonics of T-type NPC are mainly concentrated on the 5th, 7th, 11th and 13th times of the fundamental wave frequency.

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